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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,995	02/25/2004	Kenichi Kaki	566.32253CC8	9779

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EXAMINER	
ROJAS, MIDYS	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,995	KAKI ET AL.	
	Examiner	Art Unit	
	Midys Rojas	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/30/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed on January 30th, 2006, with respect to the rejection of claims 1-17 have been fully considered and are not persuasive.

Regarding Independent Claims 1 and 16, applicant argues that the prior art relied upon does not teach two separate erase operations of different non-volatile memories interleaved (or parallel) with one another. Nishi discloses sending a first and a second erase signal to different non-volatile memories. Nishi does not teach these erase signals being interleaved or parallel to one another (as claimed, "initiating the second erase command while the first erase operations is still being performed..."). This limitation is taught by Ellis.

Applicant argues that Ellis does not teach carrying out erase operations in parallel; instead, Ellis is directed to carrying out commands and ECC codes in parallel. Applicant notes that the parallel operations of Ellis are not the same as those of the instant application. However, the examiner would like to point out that Nishi already discloses the sending of two erase operations. Ellis discloses the advantage of performing memory operations in parallel (for "minimum memory read and write latency"). Therefore, since the erase commands of Nishi are memory operations as those being performed in parallel by Ellis, the combination of Nishi in view of Ellis teaches performing the two erase commands of Nishi in parallel as taught by Ellis, thus ensuring minimum memory latency. Ellis discloses the motivation for this combination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishi (5,724,544) in view of Ellis et al. (6,826,113).

Regarding Claim 1, Nishi discloses a semiconductor storage apparatus to be coupled with a system bus (connector 22, Col. 4, lines 60-67) to receive a write request accompanied with first and second sectors of data (processor sends addresses for writing... and a write signal WR, Col. 5, lines 15-64), comprising,

a plurality of nonvolatile semiconductor memories (EEPROM 30 and 40) which store said first and second sectors of data therein (address is stored by EEPROM 30 which stores supervisory data and write signal is used to store picture data in EEPROM 40, Col. 2, lines 40-52), and

a control module (20) to be coupled with said system bus (through connector 22), and coupled with said plurality of nonvolatile semiconductor memories (as seen in figure 1),

wherein said control module sends a first erase command to one of said plurality of nonvolatile semiconductor memories to initiate a first internal erase operation of data within said one of said plurality of nonvolatile semiconductor memories (when access is for rewriting data, first erase command EE1 is sent to EEPROM 30, Col. 4, lines 12-31), and

wherein, after said first erase command has been sent, said control module sends a second erase command to another of said plurality of nonvolatile semiconductor memories (a second erase signal EE2 is then sent to EEPROM 40, Col. 4, lines 12-31), different from said one of said plurality of nonvolatile semiconductor memories to which said first erase command was sent (EEPROM 30 vs. EEPROM 40), to initiate a second internal erase operation of data within said other of said plurality of nonvolatile semiconductor memories.

Nishi does not teach initiating the second erase command while the first erase operation is still being performed in the first nonvolatile memory. Ellis et al. discloses performing operations in parallel (Col. 2, lines 10-16). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Nishi to perform the erase operations in parallel as done in the system of Ellis in order to ensure minimum memory latency.

Regarding Claim 2, Nishi discloses a semiconductor storage apparatus according (1) to claim 1, further comprising:

a buffer memory (204), coupled commonly with said plurality of nonvolatile semiconductor memories (see Figure 1), which holds said first and second sectors of data as write data to be written in to said plurality of nonvolatile semiconductor memories (data buffer temporarily stores data sent from processor to the memory card... Col. 3, line 63 – Col. 4, lines 11),

wherein said control module (20) responds to said write request (by the memory controllers 208 and 210 carrying out the accessing of the EEPROMS, Col. 4, lines 12-31), carries out read operations of said first and second sectors of data as said write data from said buffer

memory and carries out write operations of said first and second sectors of data as said write data read out from said buffer memory into said plurality of nonvolatile semiconductor memories (executes write signals WR1 and WR2), wherein said write operations into said plurality of nonvolatile semiconductor memories are controlled by sending a first write command from said control module to one of said plurality of nonvolatile semiconductor memories (WR1 is sent by memory controller 208 to EEPROM 30) and by sending a second write command from said control module to another of said plurality of nonvolatile semiconductor memories different from said one to which said first write command has been sent (WR2 is sent by memory controller 210 to EEPROM 40).

Nishi does not teach initiating the second write command while the first write operation is still being performed in the first nonvolatile memory. Ellis et al. discloses performing operations in parallel (Col. 2, lines 10-16). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Nishi to perform the write operations in parallel as done in the system of Ellis in order to ensure minimum memory latency.

Regarding Claims 3-4, Nishi discloses a semiconductor storage apparatus wherein one of the EEPROMS is a flashing EEPROM (see Col. 2, lines 40-51). Nishi does not teach each of said plurality of nonvolatile semiconductor memories being comprised of a flash memory semiconductor chip. Nishi does discuss the advantages of a flashing EEPROM (Col. 1, lines 36-61). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Nishi to include two flashing EEPROMs instead of just one, thus reducing the cost of production. In exchanging the current type of EEPROM for a flashing

EEPROM, the system would have to be adjusted so that the header (or supervisory) data is stored in erasable or re-writable sections.

Regarding Claim 5, Nishi discloses a semiconductor storage apparatus (1) wherein said buffer memory (204) has a storage memory capacity corresponding to a plurality of sectors in units of one byte of data. Nishi does not teach a buffer with a capacity of 512 bytes, which is a sector capacity of a standard disk. Nishi discloses that the buffer can be used for storing data that is read out of memory section 10 (Col. 4, lines 63-67). Additionally, Nishi mentions that large capacities are necessary for the storage of picture data (Col. 4, lines 36-40). Since picture data is stored within memory section 10, and a read request would require for picture data to be read out of memory section 10 and supplied to the processor via the buffer memory 204, it would have been obvious to one of ordinary skill in the art at the time the invention was made to increase the capacity of the buffer memory in order to accommodate for the storage of picture data. Sufficiently increasing the capacity also allows for the system to store more than one picture's worth of data, thus fulfilling read requests at a faster rate.

Regarding Claims 6-7, and 12-13, Nishi discloses a semiconductor storage apparatus wherein said control module includes a processor (the processor becomes part of the control means through its connection in connector 22, Col. 4, lines 60-67).

Regarding Claims 8-9, and 14-15, Nishi discloses a semiconductor storage apparatus wherein said control module (20) further includes an address controller (address identification 206, Col. 4, lines 1-11).

Regarding Claims 10-11, Nishi discloses a semiconductor storage apparatus wherein one of the EEPROMS is a flashing EEPROM (see Col. 2, lines 40-51). Nishi does not teach each of said plurality of nonvolatile semiconductor memories being comprised of a flash memory semiconductor chip. Nishi does discuss the advantages of a flashing EEPROM (Col. 1, lines 36-61). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Nishi to include two flashing EEPROMs instead of just one, thus reducing the cost of production. In exchanging the current type of EEPROM for a flashing EEPROM, the system would have to be adjusted so that the header (or supervisory) data is stored in erasable or re-writable sections.

Additionally, the system of Nishi teaches buffer memory (204) that has a storage memory capacity corresponding to a plurality of sectors in units of one byte of data. Nishi does not teach a buffer with a capacity of 512 bytes, which is a sector capacity of a standard disk. Nishi reveals that the buffer can be used for storing data that is read out of memory section 10 (Col. 4, lines 63-67). Additionally, Nishi mentions that large capacities are necessary for the storage of picture data (Col. 4, lines 36-40). Since picture data is stored within memory section 10, and a read request would require for picture data to be read out of memory section 10 and supplied to the processor via the buffer memory 204, it would have been obvious to one of ordinary skill in the art at the time the invention was made to increase the capacity of the buffer memory in order to

accommodate for the storage of picture data. Sufficiently increasing the capacity might also allow for the system to store more than one picture's worth of data, thus fulfilling read requests at a faster rate.

Claim 16 is rejected using the same rationale as that used in Claim 1.

Regarding Claim 17, Nishi discloses a semiconductor storage apparatus wherein said control module (system controller 212, which is part of control module 20) carries out a status polling operation in an order of said nonvolatile semiconductor memories to which said control module sent said erase commands after said control module sent said erase commands to all of said nonvolatile semiconductor memories ("continuously sends a signal BUSY to the processor to report that processing is underway in the memory card", Col. 4, lines 32-38).

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Rojas whose telephone number is (571) 272-4207. The examiner can normally be reached on M-F 5:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 1, 2006

Midys Rojas
Midys Rojas
Examiner
Art Unit 2185

MR

Pierre Vital
PIERRE VITAL
PRIMARY EXAMINER